

EL465854335US

EL169867345

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR LETTERS PATENT

* * * * *

Physical Vapor Deposition Targets, Conductive
Integrated Circuit Metal Alloy Interconnections,
Electroplating Anodes, And Metal Alloys For Use
As A Conductive Interconnection In An Integrated
Circuit

* * * * *

INVENTORS

Shozo Nagano
Hinrich Hargarter
Jianxing Li
Jane Buehler

ATTORNEY'S DOCKET NO. AL41-003

1 **Physical Vapor Deposition Targets, Conductive Integrated Circuit**
2 **Metal Alloy Interconnections, Electroplating Anodes, And Metal Alloys**
3 **For Use As A Conductive Interconnection In An Integrated Circuit**

4 **TECHNICAL FIELD**

5 This invention relates to physical vapor deposition targets, to
6 conductive integrated circuit metal alloy interconnections, and to
7 electroplating anodes.

8
9
10 **BACKGROUND OF THE INVENTION**

11 Aluminum and its alloys are common metal materials used in
12 metal interconnects in the fabrication of integrated circuitry on
13 semiconductor wafers. Yet as circuitry density increases and operating
14 speed increases, aluminum's electrical resistance is expected to prevent
15 its use in many next generation circuits. Copper has been proposed as
16 a strong candidate to replace aluminum and its alloys due to copper's
17 low bulk resistivity of 1.7 microohms.cm at near 100% purity (i.e.,
18 greater than 99.999% copper). Further, it has electromigration
19 resistance compared to that of aluminum and its alloys of about
20 10 times or greater.

21 One problem associated with pure copper interconnects concerns
22 abnormal grain growth or thermal stability in the deposited film.
23 Further, such abnormal and undesired grain growth can reduce the film's
24 electromigration resistance. Low thermal stability is defined as, and

1 abnormal grain growth is characterized by, a tendency of the individual
2 crystal grains within copper to grow when exposed to a certain
3 temperature. The higher the temperature at which a material
4 recrystallizes or starts to grow larger grains, the higher the thermal
5 stability of the material.

6 Elemental copper and its alloys can be deposited in integrated
7 circuitry fabrication using a number of techniques, including chemical
8 vapor deposition, physical vapor deposition and electrochemical
9 deposition, such as electroplating. Ideally when deposited, the copper
10 comprising sputtering target will have substantially uniform microstructure,
11 a fine grain size, and preferred crystal orientation in order to achieve
12 desired sputtering performance and resultant thin film formation and
13 properties.

14 15 16 SUMMARY

17 The invention includes conductive integrated circuit metal alloy
18 interconnections, physical vapor deposition targets and electroplating
19 anodes. In one implementation, a physical vapor deposition target
20 includes an alloy of copper and silver, with the silver being present in
21 the alloy at from less than 1.0 at% to 0.001 at%. In one
22 implementation, a physical vapor deposition target includes an alloy of
23 copper and silver, with the silver being present in the alloy at from
24 50 at% to 70 at%. In one implementation, a physical vapor deposition

PATENT OFFICE

1 target includes an alloy of copper and tin, with tin being present in the
2 alloy at from less than 1.0 at% to 0.001 at%.

3 In one implementation, a conductive integrated circuit metal alloy
4 interconnection includes an alloy of copper and silver, with the silver
5 being present in the alloy at from less than 1.0 at% to 0.001 at%.

6 In one implementation, a conductive integrated circuit metal alloy
7 interconnection includes an alloy of copper and silver, with the silver
8 being present in the alloy at from 50 at% to 70 at%. In one
9 implementation, a conductive integrated circuit metal alloy interconnection
10 includes an alloy of copper and tin, with tin being present in the alloy
11 at from less than 1.0 at% to 0.001 at%.

12 In one implementation, an electroplating anode includes an alloy
13 of copper and silver, with the silver being present in the alloy at from
14 less than 1.0 at% to 0.001 at%. In one implementation, an
15 electroplating anode includes an alloy of copper and silver, with the
16 silver being present in the alloy at from 50 at% to 70 at%. In one
17 implementation, an electroplating anode includes an alloy of copper and
18 tin, with tin being present in the alloy at from less than 1.0 at% to
19 0.001 at%.

20 In other implementations, other useable copper alloys in physical
21 vapor deposition targets, conductive integrated circuit metal alloy
22 interconnections, and electroplating anodes include an alloy of copper
23 and one or more other elements, the one or more other elements being
24 present in the alloy at a total concentration from less than 1.0 at% to

1 0.001 at% and being selected from the group consisting of Be, Ca, Sr,
2 Ba, Sc, Y, La, Ce, Pr, Nd, Pm, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb,
3 Lu, Ti, Zr, Hf, Zn, Cd, B, Ga, In, C, Se, Te, V, Nb, Ta, Cr, Mo, W,
4 Mn, Tc, Re, Fe, Ru, Os, Co, Rh, Ni, Pd, Pt, Au, Tl, and Pb. An
5 electroplating anode is formed to comprise one or more of the above
6 alloys.

7 In other implementations, the invention contemplates metal alloys
8 for use as a conductive interconnection in an integrated circuit.
9
10

11 BRIEF DESCRIPTION OF THE DRAWINGS

12 Preferred embodiments of the invention are described below with
13 reference to the following accompanying drawings.

14 Fig. 1 is a diagrammatic sectional view of a physical vapor
15 deposition target system in accordance with an aspect of the invention.

16 Fig. 2 is a diagrammatic sectional view of an electroplating system
17 incorporating an electroplating anode in accordance with an aspect of
18 the invention.

19 Fig. 3 is a cross-sectional view of a semiconductor wafer fragment
20 comprising integrated circuitry including a conductive metal alloy
21 interconnection in accordance with an aspect of the invention.
22
23
24

1 DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

2 This disclosure of the invention is submitted in furtherance of the
3 constitutional purposes of the U.S. Patent Laws "to promote the
4 progress of science and useful arts" (Article 1, Section 8).

5 The present invention includes novel physical vapor deposition
6 targets comprising alloys of copper and silver, and comprising alloys of
7 copper and tin. The invention also contemplates conductive integrated
8 circuit interconnections comprised of such metal alloys, and whether
9 deposited utilizing the inventive physical vapor deposition targets, by
10 chemical vapor deposition or by other methods. The invention includes
11 electroplating anodes comprising alloys of copper and silver, and
12 comprising alloys of copper and tin. The invention also includes
13 physical vapor deposition targets, conductive integrated circuit
14 interconnections, and electroplating anodes comprising other copper
15 alloys. The invention also contemplates metal alloys for use as a
16 conductive interconnection in an integrated circuit, by way of example
17 only as might be used as raw material for producing physical vapor
18 deposition targets or electroplating anodes.

19 In one implementation, a physical vapor deposition target
20 comprises an alloy of copper and silver, with the silver being present
21 in the alloy at from less than 1.0 at% to 0.001 at%, and more
22 preferably at from 0.005 at% to 0.1 at%. An aspect of the invention
23 also includes a conductive integrated circuit metal alloy interconnection
24 comprising this alloy of copper and silver. Preferably, such

Patented 11-13-60

1 interconnection will have higher electromigration resistance than copper
2 of a purity greater than 99.999% of the same grain size. Further
3 preferably, the alloy will have greater thermal stability to grain size
4 retention and crystal orientation retention than copper of a purity of
5 greater than 99.999% of the same grain size. Further preferably, very
6 near the pure copper electrical conductivity is ideally achieved.
7 Preferably when the interconnection is deposited from a sputtering
8 target, the alloy offers very stable sputtering target microstructure and
9 texture. A thermally stabilized target of this alloy can offer improved
10 sputtering performance and resultant thin film properties within the
11 circuitry. Regardless and when deposited from chemical vapor
12 deposition or other methods, the alloy offers higher electromigration
13 resistance while maintaining very near the pure copper electrical
14 conductivity. Silver can form uniformly fine precipitates in the
15 microstructure in the form of elemental precipitates.

16 In another aspect of the invention, the physical vapor deposition
17 target comprises an alloy of copper and silver, with silver being present
18 in the alloy at from 50 at% to 70 at%, more preferably at between
19 55 at% and 65 at%, and most preferably at about 60 at%. The
20 invention also contemplates a conductive integrated circuit metal alloy
21 interconnection comprising this alloy of copper and silver, whether
22 deposited by physical vapor deposition, chemical vapor deposition or
23 other methods. Most preferably, the resultant alloy as formed in the
24 circuit has higher electromigration resistance than copper of a purity of

1 greater than 99.999% of the same grain size. Further preferably, the
2 alloy interconnection preferably has greater thermal stability to grain size
3 retention and crystal orientation retention than copper of a purity of
4 greater than 99.999% of the same grain size.

5 Silver is a very desirable doping element in copper for physical
6 vapor deposition targets and conductive integrated circuitry metal alloy
7 interconnections, as it has a similar electrical resistivity with copper and
8 forms essentially no solid solution with copper. Accordingly, a
9 copper-silver alloy can be largely represented as a mechanical mixture
10 of silver grains and copper grains. Due to this structure and mixture,
11 a copper-silver alloy has minimum electrical resistivity increase over that
12 of pure copper even at high-level silver concentrations. Further, it is
13 reported that the lowest electrical resistivity of copper-silver alloys is
14 close to the eutectic composition, which is at about copper at 40 at%,
15 silver at 60 at%, and is only about 10% above the resistivity of pure
16 copper. Accordingly, a considerably reduced or lower reflow
17 temperature can be achieved using a copper alloy at or about the 60
18 at% silver eutectic point for the alloy. This will result in a melt
19 temperature of about 780°C, which is considerably lower than a pure
20 copper melt temperature of about 1085°C, and is only about 120°C
21 above the melt temperature for aluminum and alloys thereof commonly
22 presently used in conductive integrated circuit interconnections.
23 Accordingly, the low-melt temperature of the eutectic alloy presents an
24

1 opportunity for low temperature reflow after thin film deposition for
2 small via and deep trench-fill applications.

3 This particular application could have a profound impact on thin
4 film deposition. With the ever shrinking device feature size and
5 integrated circuitry design rules, one of the bottlenecks for thin film
6 deposition is the complete filling of small via and trenches. Pressure
7 or temperature-assisted film deposition has been adopted to leverage the
8 difficulty of small via and trench-fill in aluminum metallization.
9 However, high pressure is not well-compatible with conventional
10 integrated circuitry processes, and therefore has not been very well
11 accepted by the industry. Accordingly, predominantly high temperature
12 processing has been used in most applications. Yet for copper
13 metallization, the temperature-assisted deposition is not expected to be
14 practical due to its high melt temperature. Yet, copper-silver alloys at
15 the preferred composition range between 50 at% and 70 at% silver, and
16 even more preferably at around the eutectic point of 60 at% silver,
17 may provide significant processing advantages in using copper alloys.

18 In another aspect of the invention, a physical vapor deposition
19 target comprises an alloy of copper and tin, with tin being present in
20 the alloy at from less than 1.0 at% to 0.001 at%, and more preferably
21 at from 0.01 at% to 0.1 at%. An aspect of the invention also
22 contemplates conductive integrated circuitry metal alloy interconnections
23 comprising this alloy. Preferably, such interconnections will have higher
24 electromigration resistance than copper of a purity of greater than

99.999% of the same grain size. Further preferably, such interconnections will have greater thermal stability to grain size retention and crystal orientation retention than copper of a purity of greater than 99.999% of the same grain size. Further preferably, the interconnections will have an electrical resistivity of less than 1.8 microohms.cm. Tin can form uniformly fine precipitates in the microstructure in the form of intermetallic compound precipitates.

A series of copper alloys were prepared using conventional vacuum induction melt and air melt methods. A high purity copper (purity of 99.9998% (5N8)) was used as a reference, as well as the starting material for the copper alloys described above. Different levels of silver and tin were doped into the reference copper to obtain the copper alloys. Chemical analysis was taken from the as-cast samples using glow discharge mass spectroscopy (GDMS). Thermal stability was evaluated using hardness, grain size, and texture (grain orientation) analysis at different temperatures. Electrical resistivity was measured using bulk samples at room temperature.

The detailed results are shown in the tables below, with all ppm values being in weight percent.

Material	Electrical Resistivity ($\mu\Omega\cdot\text{cm}$)
Pure Cu (5N8)	1.70
Cu w/ 16 ppm Sn	1.71
Cu w/ 530 ppm Sn	1.69
Cu w/ 135 ppm Ag	1.82
Cu w/ 145 ppm Ag	1.75
Cu w/ 385 ppm Ag	1.75

Material	Recrystallization Temperature ($^{\circ}\text{C}$)
Pure Cu (5N8)	150
Cu w/ 350 ppm Sn	250
Cu w/ 530 ppm Sn	300
Cu w/ 145 ppm Ag	350
Cu w/ 385 ppm Ag	400

Material	Grain Size Retention Temperature ($^{\circ}\text{C}$)	Texture Retention Temperature ($^{\circ}\text{C}$)
Pure Cu (5n8)	350 (grain size $30\mu\text{m}$)	150
Cu w/ 530 ppm Sn	>400 (grain size $20\mu\text{m}$)	300
Cu w/ 385 ppm Ag	>400 (grain size $20\mu\text{m}$)	400

1 The above reduction-to-practice examples show tin and
2 silver-copper alloys having approximately the same electrical resistivity
3 as pure copper. Further, such copper alloys demonstrate improved
4 thermal stability and refined grain structure.

5 Both silver and tin have negligible solid solubility in copper at
6 room temperature. Accordingly, almost all of the doped silver and tin
7 preferably precipitates out of the copper matrix once the alloy is
8 solidified. A preferred result is a virtually clean copper matrix with a
9 small amount of silver or CuSn_3 intermetallic compounds. Preferably,
10 there is little copper lattice distortion in very small amount of
11 precipitates, leaving the electrical resistivity very close to pure copper.
12 This trend should result where the doping element does not form solid
13 solution with copper, and its amount is less than 1 at% silver or tin.

14 The invention also contemplates use of other copper alloys in
15 physical vapor deposition targets, conductive integrated circuit
16 interconnections, and electroplating anodes. These materials include
17 elements which have low room temperature solid solubility and uniformly
18 distributed fine precipitates in the microstructure, much like silver and
19 tin. One class of elements forms intermetallic compound precipitates
20 in the microstructure. These include Be, Ca, Sr, Ba, Sc, Y, La, Ce,
21 Pr, Nd, Pm, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, Lu, Ti, Zr, Hf,
22 Zn, Cd, B, Ga, In, C, Se, and Te. In accordance with an aspect of
23 the invention, physical vapor deposition targets, conductive integrated
24 circuit interconnections, and electroplating anodes are comprised of an

1 alloy of copper and one or more other elements, with the one or more
2 other elements being present in the alloy at a total concentration from
3 less than 1.0 at% to 0.001 at% and being selected from the group
4 consisting of Be, Ca, Sr, Ba, Sc, Y, La, Ce, Pr, Nd, Pm, Sm, Eu, Gd,
5 Tb, Dy, Ho, Er, Tm, Yb, Lu, Ti, Zr, Hf, Zn, Cd, B, Ga, In, C, Se,
6 and Te. Such copper alloys are expected to have higher
7 electromigration resistance than copper of a purity of greater than
8 99.999% of the same grain size. Further, such copper alloys are
9 expected to have greater thermal stability to grain size retention and
10 crystal orientation retention than copper of a purity of greater than
11 99.999% of the same grain size.

12 Another class of elements forms element precipitates in the
13 microstructure. These include V, Nb, Ta, Cr, Mo, W, Mn, Tc, Re, Fe,
14 Ru, Os, Co, Rh, Ni, Pd, Pt, Au, Tl, and Pb. In accordance with an
15 aspect of the invention, physical vapor deposition targets, conductive
16 integrated circuit interconnections, and electroplating anodes are
17 comprised of an alloy of copper and one or more other elements, with
18 the one or more other elements being present in the alloy at a total
19 concentration from less than 1.0 at% to 0.001 at% and being selected
20 from the group consisting of V, Nb, Ta, Cr, Mo, W, Mn, Tc, Re, Fe,
21 Ru, Os, Co, Rh, Ni, Pd, Pt, Au, Tl, and Pb. / Such copper alloys are
22 expected to have higher electromigration resistance than copper of a
23 purity of greater than 99.999% of the same grain size. Further, such
24 copper alloys are expected to have greater thermal stability to grain size

1 retention and crystal orientation retention than copper of a purity of
2 greater than 99.999% of the same grain size.

3 Fig. 1 diagrammatically depicts a sputtering system comprising a
4 sputtering assembly 20 and a wafer 22 to be sputter deposited upon.
5 Sputtering assembly 20 comprises a main sputtering target 24 adhered
6 to a backing plate 26 by conventional or yet-to-be developed methods.
7 Sputtering assembly 20 also includes an RF sputtering coil 28 received
8 intermediate main target 24 and substrate 22. One or both of main
9 target 24 and RF sputtering coil 28 is fabricated to comprise one or
10 more of the above alloys.

11 In one aspect, the invention also contemplates use of one or
12 more of the above alloys as an electroplating anode. Fig. 2
13 diagrammatically depicts but an exemplary electroplating system 30
14 comprising a liquid reservoir 31. A substrate 32 to be deposited upon
15 and an electroplating anode 34 are received within a suitable plating
16 solution within reservoir 31 opposite one another. Substrate 32 and
17 anode 34 are electrically interconnected with one another through a
18 suitable power source 36 configured to enable substrate 32 to function
19 as a cathode, and thereby deposit material from electroplating anode 34
20 onto substrate 32.

21 Fig. 3 illustrates but an exemplary semiconductor wafer fragment
22 indicated generally with reference numeral 10. Such comprises a bulk
23 semiconductive substrate 12 having an electrically conductive diffusion
24 region 14 formed therein. An electrically insulating layer 16 is formed

over substrate 12 and a contact opening 18 has been formed therethrough over diffusion region 14. Such has been plugged with an electrically conductive plugging material 25, which preferably comprises one or more of the alloys as described above. Diffusion barrier or adhesion layers (not shown) might also, of course, be utilized relative to contact opening 18. An electrically conductive line 26 has been deposited and patterned over and in electrical connection with conductive plugging material 25. Interconnect line 26 also preferably comprises one or more of the above-described alloys. Components 26 and 25 constitute exemplary conductive integrated circuit metal alloy interconnections preferably comprising one or more of the alloys described herein. Such might comprise different materials as depicted by the different section lines, or constitute the same material throughout. Other constructions are of course contemplated.

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.